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(54) **Low sheet resistivity composite conductor gate MOS device**

(57) The gate electrode of a MOS device comprises a layer 26 of a highly conductive material interposed between two polysilicon layers 14, 18. This provides a gate electrode of reduced sheet resistivity. The highly conductive material may be a metal silicide formed by depositing a layer of a metal alloy or metal(eg Ti,Ta,W,Pt or Mo) on the first polysilicon layer 14, covering with the second polysilicon layer 18 and heating to react the metal with the polysilicon. Alternatively a metal silicide layer may be formed by direct deposition.

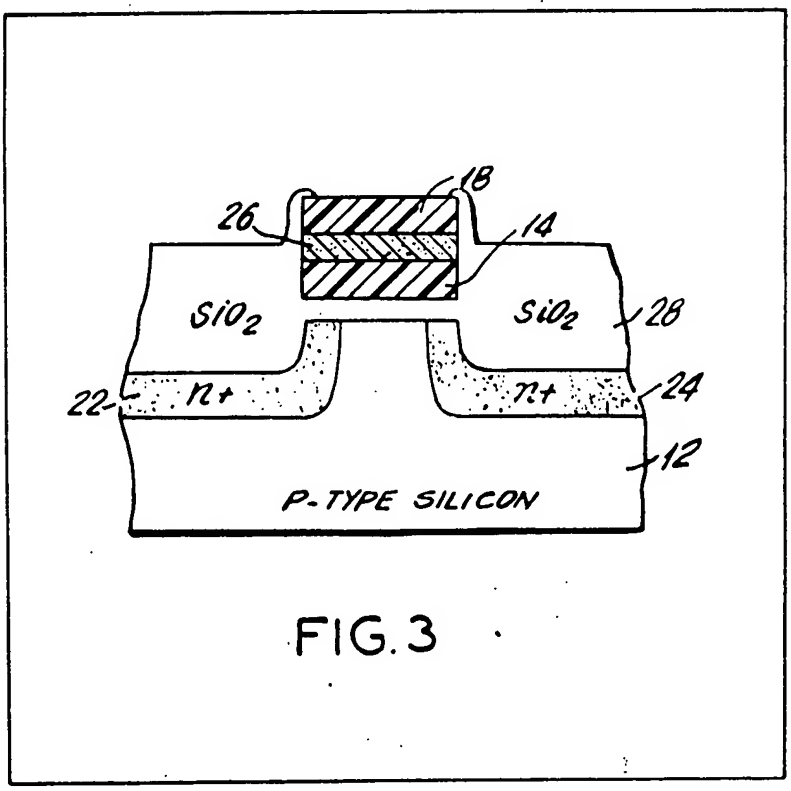


FIG. 3

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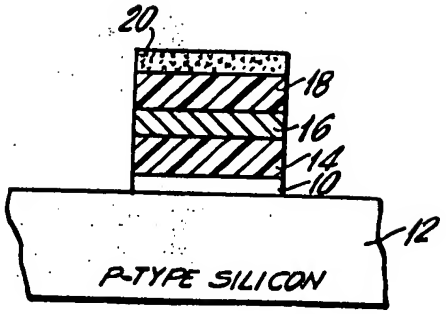


FIG. 1

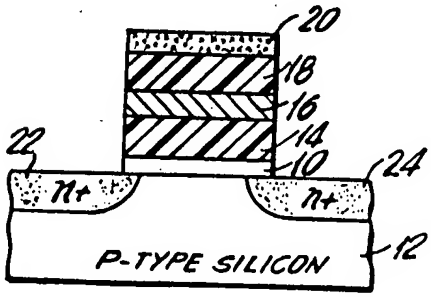


FIG. 2

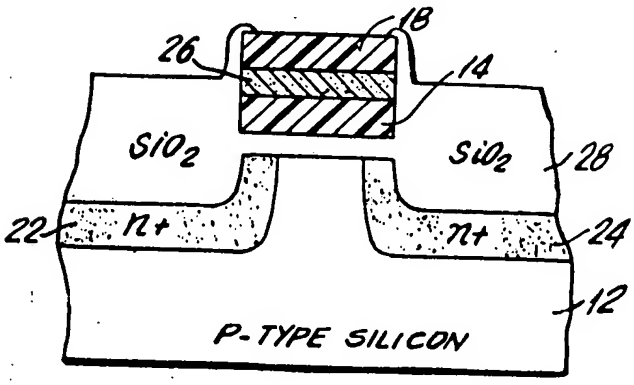


FIG. 3

SPECIFICATION

**Low sheet resistivity composite conductor gate MOS device**

The present invention relates generally to MOS devices, and more particularly to silicon-gate MOS devices.

Silicon gate MOS devices in which a doped polycrystalline silicon, or polysilicon, layer serves as the gate electrode are widely used in a wide variety of MOS integrated circuits, such as read-only memories and random-access memories. The speed of silicon-gate MOS devices has heretofore been limited by, among other things, the relatively high polysilicon sheet resistivity, which is typically in the order of 15 to 40 ohms per square. Since the speed of operation of an MOS circuit is dependent on RC time constants within the circuit, the relatively high level of sheet resistivity of the conventional silicon-gate devices limits the speed of operation of integrated circuits which contain these devices.

Although the desirability of reducing the sheet resistivity of silicon-gate MOS devices to increase the operating speed of these devices has long been recognized in the semiconductor industry, a successful and practical means of reducing the sheet resistivity, thereby reducing the RC time constant and increasing operating speed, has thus far not been achieved.

In an attempt to reduce sheet resistivity of the material used for the gate electrode in MOS devices, refractory metals or refractory silicides such as molybdenum, titanium disilicide, tantalum disilicide, and molybdenum disilicide have been considered for use as materials in the gate structures of MOS integrated circuit structures. Reports on these considerations have been presented by A. T. Sinha et al at the IEEE Reliability Physics Symposium, in April 1980, entitled "Generic MOS Reliability of the High Conductivity $TaSi_2$/n+ Poly-Si Gate Structure", and by S. P. Murarka, at the IEEE International Electron Devices meeting in December, 1979, entitled "Refractory Silicides for Low Resistivity Gates and Interconnects." Although the use of the materials proposed in these reports in MOS devices provides a reduction in sheet resistivity as compared to heavily-doped polysilicon, they are often difficult to deposit and to etch accurately, and often degrade the electrical characteristics of the MOS integrated circuits which include these materials in their gate structures by introducing additional deleterious mechanisms, such as instabilities, into the devices.

It is, therefore, an object of the invention to provide an MOS silicon gate device capable of operating at higher speeds than has thus far been possible.

It is a further object of the invention to provide an MOS structure of the type described which can be fabricated without the need for additional photolithographic operations.

It is a further object of the invention to provide an improved conducting gate material which can be formed by the use of deposition and etching techniques, the characteristics of which are known and understood by MOS engineers.

It is a general object of the invention to provide an MOS structure which provides the advantages of conventional silicon gate technology while providing a substantial reduction in sheet resistivity and a concomitant increase in device operating speed.

In accordance with the invention, a conductive layer of a metal or metal alloy is interposed or "sandwiched" between two layers to form a composite gate electrode of an MOS device. When the material of the intermediate layer is a metal, the sandwich is heated so that the metal in the intermediate layer reacts with the overlying and underlying polysilicon layers to form a silicide of the metal. The gate electrode structure fabricated in this manner, in which a conductive metal silicide is interposed between two polysilicon layers, has a significantly reduced sheet resistivity.

To the accomplishment of the above and any further objects that may hereinafter appear, the present invention relates to a silicon-gate MOS device and the method for its manufacture, substantially as defined in the appended claims, and as described in the following specification as considered together with the accompanying drawing in which:

*Figure 1* is a cross section of an MOS device during an intermediate state of its fabrication in accordance with the present invention;

*Figure 2* is a cross section of the MOS device of Figure 1 at a later stage of its fabrication; and

*Figure 3* is a cross section of the device at a still later stage of its fabrication.

In Figure 1, there is shown an MOS device after the completion of an early stage of its fabrication. As therein shown, a thin (typically 1,000Å) insulating layer 10 of a silicon dioxide is formed in a conventional manner over a substrate 12 of silicon, here shown for purposes of illustration, as being of p-type conductivity.

A highly doped polycrystalline silicon layer 14 is deposited over the thin oxide layer 10. The thickness of this highly doped polycrystalline silicon layer is, typically, between 500Å and 2,500Å, and it is typically doped with n-type impurities such as arsenic or antimony. Next, a thin layer 16, which is advantageously between 500Å and 1,500Å in thickness, of a metal such as titanium, tantalum, tungsten, platinum or molybdenum is deposited over polysilicon layer 14. The material chosen for use in layer 16 is preferably a metal having the property of being able to combine with polysilicon at high temperatures to form a conducting silicide. The material of layer 16 may also be an alloy or compound of a metal, such as titanium disilicide, which has comparable characteristics, but does not need to further react with the polysilicon to form the silicide of the metal. In the embodiment of the invention herein described, the material of layer 16 is titanium which may be deposited onto polysilicon layer 14 by electron-beam evaporation.

Immediately following the deposition of the titanium layer 16, a second polysilicon layer 18, which may be doped with an n-type impurity such as arsenic, antimony, or phosphorus, is deposited over

the titanium layer 16 in a conventional manner to a thickness in the order of 2,000Å, after which a masking layer 20 of silicon nitride of a thickness in the order of 1,500Å is deposited over the polysilicon layer using plasma deposition techniques at temperatures lower than 500°C.

Following the deposition of the nitride layer 20, a layer of photoresist material (not shown) is deposited over the multilayered structure and is thereafter exposed and developed to a desired pattern through the use of conventional photolithographic techniques. Next, using the patterned photoresist as a mask, the underlying silicon nitride layer 20 is etched through conventional chemical etching or plasma etching techniques and the remaining photoresist is stripped off. Then, using the patterned layer of silicon nitride as a mask, the underlying layers of polysilicon, titanium, polysilicon and silicon dioxide are etched away, one or more at a time using conventional chemical etching, plasma etching, or ion-milling techniques, down to the silicon substrate 12. The structure that is achieved as a result of these steps is shown in Figure 1. When ion-milling techniques are employed, it may be desirable to subject the structure to high temperatures (which would result in the formation of the silicide) before the ion-milling procedure is performed.

The structure of Figure 1 is then subjected to a diffusion or implantation operation in which the multilayered structure of Figure 1 operates as a mask to achieve a self-aligned gate structure, whereby spaced n+−type source and drain regions 22 and 24 are formed in the upper surface of substrate 12, as shown in Figure 2. During, or before, this operation, the structure is typically exposed to temperatures in excess of 700°C in an inert ambient such as dry nitrogen for a sufficient period of time to allow the metal of the intermediate layer 16, here titanium, to react with the polycrystalline silicon material directly above and below it to form a silicide of the metal, here titanium disilicide 26 (Figure 2).

In the event that titanium disilicide or other conductive disilicide or alloy of a metal is employed as the starting material for layer 16, no significant further reaction would occur between that material and the polysilicon layers, although the resulting structure would be comparable in that it would comprise the layer of conductive silicide covered by and overlying a polysilicon layer.

The titanium disilicide layer 26 in the resulting "sandwich" gate electrode is advantageous as it behaves in a manner similar to a refractory metal, is highly conductive, and oxidizes at a rate comparable to the polysilicon.

Thereafter, the structure of Figure 2 is subjected to a local oxidation operation in which the silicon nitride layer 20 is used as a mask. In this operation, the silicon substrate 12 is oxidized so as to form a thick oxide layer 28 of a thickness in the order of 10,000Å, which extends below and surrounds the composite conducting gate electrode. The side walls of the composite conducting material are also oxidized during this operation.

Thereafter, the silicon nitride layer 20 is removed resulting in the structure shown in Figure 3. The structure includes a three-layer composite gate electrode made up of the two polysilicon layers and the intermediate titanium disilicide layer. Preferably, an additional diffusion may be subsequently performed in the exposed upper (polysilicon) surface of the composite layer, and an additional oxidation step may be performed to the upper surface of the polysilicon layer, thereby to provide a thin oxide layer (not shown), which provides electrical isolation between the polysilicon layer and a subsequently formed, overlying metal interconnection layer (also not shown). Alternately, a similar, but thicker, oxide layer may be chemically deposited to provide such electrical isolation. The resulting MOS structure is then completed according to conventional fabrication techniques.

The MOS device constructed according to the present invention, as described in the foregoing exemplary embodiment, provides a low-sheet resistivity composite gate electrode which is substantially equivalent in all other ways to a conventional polysilicon gate electrode. The composite gate electrode of the invention includes a highly conductive metal silicide layer sandwiched between polysilicon layers. However, it differs from the conventional silicon-gate MOS device in that it provides a remarkably low value of sheet resistivity, in the order of between 0.5 and 5.0 ohms per square, as compared to conventional doped polysilicon gate structures in which the sheet resistivity of the doped polysilicon is typically between 15 and 40 ohms per square. The reduced sheet resistivity achieved in the MOS device of the present invention significantly improves the speed of the MOS device and is thus highly advantageous for use in many applications of MOS devices, such as random-access memories, in which speed of operation is of particular importance.

In addition, the gate-insulator interface between the first polysilicon layer 14 and the oxide layer 10 is a polysilicon-$SiO_2$ interface and all contacts made to the conductive gate will be to the upper polysilicon layer 18. Since the characteristics of the polysilicon-$SiO_2$ gate-insulator interface and of the aluminum connections to the overlying polysilicon layer are known to the MOS process engineer, the improved gate electrode structure of the invention can be readily utilized by the manufacturer of MOS devices without the need for additional considerations.

Although the invention has been specifically described for purposes of example with titanium used as the starting material for the conductive layer interposed between the two polysilicon layers, other metals and alloys may also be used which meet the requirements for this material as set forth above. It will thus be appreciated that modifications may be made in the embodiment of the invention hereinabove described without necessarily departing from the spirit and scoope of the invention.

## CLAIMS

1. A method of fabricating an MOS device which comprises the steps of providing a substrate, forming on a surface of said substrate a thin insulating layer, depositing on said insulating layer a first layer

of polysilicon, depositing on said first polysilicon layer an electrically conductive layer of a material capable of reacting with polysilicon when heated to an elevated temperature to form a conductive silicide, depositing a second polysilicon layer over said conductive layer, and thereafter heating said structure to cause polysilicon in said first and second polysilicon layers to react with the material of said conductive layer to form a silicide of the material of said conductive layer.

2. The method of Claim 1, in which said conductive layer is formed of a metal.

3. The method of Claim 2, in which said conductive layer is a metal selected from the group consisting of titanium, tantalum, tungsten, platinum, and molybdenum.

4. The method of Claim 1, further comprising the step of oxidizing said substrate to form a thick oxide layer which surrounds said conductive layer and said first and second polysilicon layers.

5. A method of fabricating an MOS device which comprises the steps of providing a silicon substrate, forming a thin oxide layer over said substrate, depositing a first doped polysilicon layer over said thin oxide layer, depositing a conductive layer over said first polysilicon layer, depositing a second doped polysilicon layer over said conductive layer, and selectively removing portions of said oxide layer, said conductive layer, and said first and second polysilicon layers, thereby to form a composite three-layer gate structure in which said conductive layer is interposed between said first and second polysilicon layers.

6. The method of Claim 5, in which said conductive layer is formed of a metal.

7. The method of Claim 5, in which said conductive layer is a metal selected from the group consisting of titanium, tantalum, tungsten, platinum, and molybdenum.

8. The method of Claim 6, further comprising the step of heating said gate structure in an inert ambient to cause said metal to react with the polysilicon of said first and second polysilicon layers to form a silicide of said metal.

9. The method of Claim 8, in which said conductive layer is a metal selected from the group consisting of titanium, tantalum, tungsten, platinum, and molybdenum.

10. The method of Claim 5, in which said conductive layer is formed of a metal silicide.

11. The method of Claim 5, further comprising the steps of oxidizing said substrate to form a thick oxide layer which surrounds said conductive layer and said first and second polysilicon layers.

12. An MOS transistor device comprising a substrate, spaced source and drain regions formed in a surface of said substrate, an oxide layer overlying said substrate surface and extending between said source and drain regions, and a gate electrode structure overlying said oxide layer, said gate electrode structure comprising a first doped polysilicon layer overlying said oxide layer, an electrically conductive layer overlying and in contact with said first polysilicon layer, and a second polysilicon layer overlying and in contact with said conductive layer.

13. The MOS device of Claim 12, in which said conductive layer is a silicide of a metal selected from the group consisting of titanium, tantalum, tungsten, platinum, and molybdenum.

14. A method of fabricating an MOS device, substantially as herein described with reference to the accompanying drawings.

15. An MOS device substantially as herein described with reference to the accompanying drawings.

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